Addendum to Domain Personal Workstations and Servers Hardware Architecture Handbook

Order No. 019411-A00

UNIX is a registered trademark of UNIX System Laboratories Inc.

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

Hewlett-Packard assumes no responsibility for the use or reliability of its software on equipment that is not furnished by Hewlett-Packard.

RESTRICTED RIGHTS LEGEND. Use, duplication, or disclosure by government is subject to restrictions as set forth in subdivision (c) (1) (ii) of the Rights in Technical Data and Computer Software Clause at DFARS 252.227.7013. Hewlett-Packard Co., 3000 Hanover St., Palo Alto, CA 94304

10 9 8 7 6 5 4 3 2 1

Preface

This addendum contains corrections and additions to information in the *Domain Personal Workstations and Servers Hardware Architecture Handbook (Order Number 007861–A01)* manual.

Please use the information in this addendum in place of existing information in the *Domain Personal Workstations and Servers Hardware Architecture Handbook* manual as indicated.

Replace the figure on page 1–6 with the following figure.

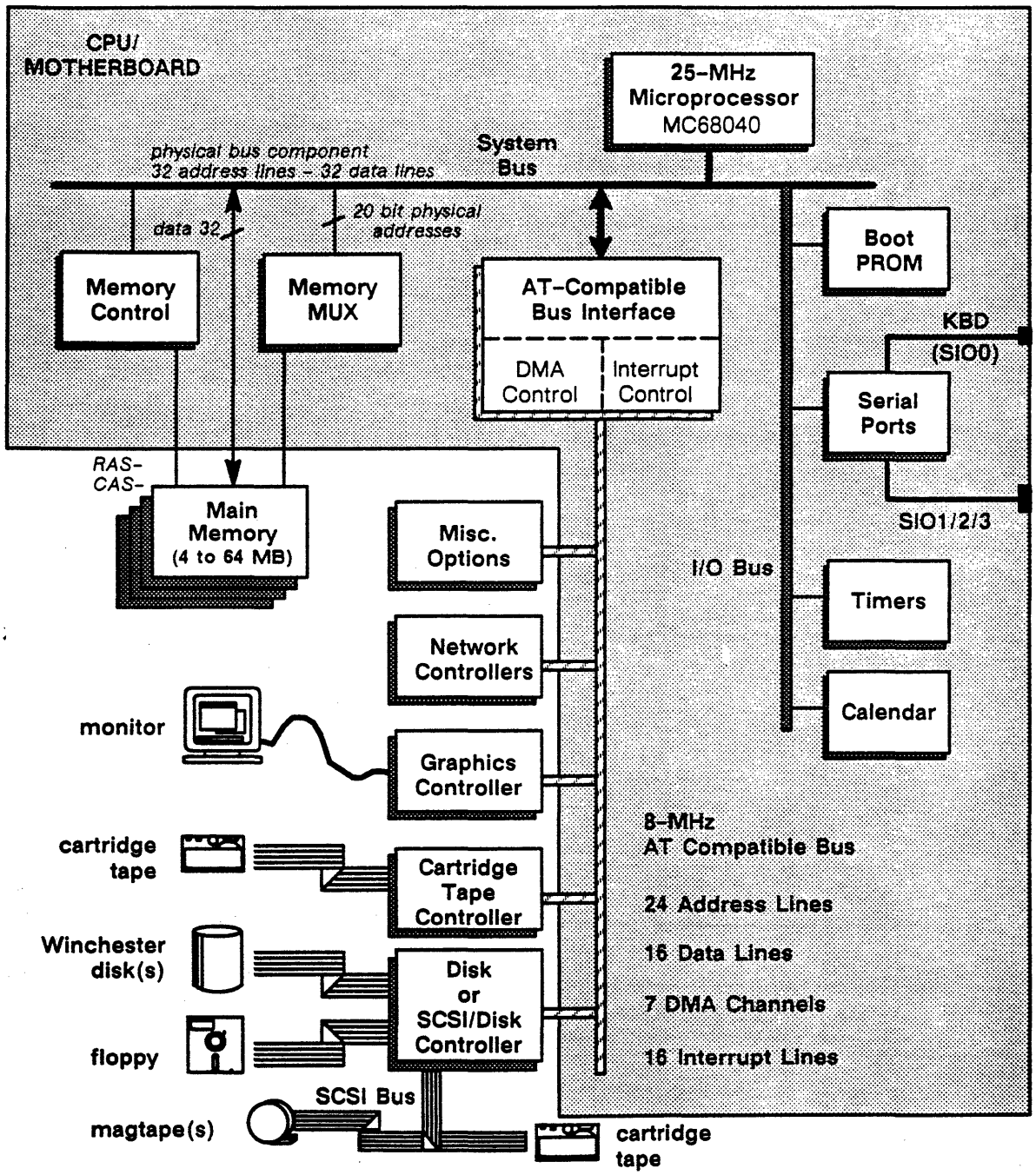


Figure 1–5. DS5500 System

Replace the Table on page 2–7 with the following table.

Table 2–5. DS5500 256–MB Physical Address Space Allocation

Physical Address	Function
000000–00FFFF	BOOT PROM
010000–0100FF	CPU STATUS REGISTER
010100–0101FF	CPU CONTROL REGISTER
010200–0102FF	CACHE STATUS REGISTER
010400–0104FF	SIO CONTROLLER No. 1
010500–0105FF	SIO CONTROLLER No. 2
010800–0108FF	INTERVAL TIMER
010900–0109FF	CALENDAR
010C00–010CFF	DMA CONTROLLER No. 1
010D00–010DFF	DMA CONTROLLER No. 2
011000–0110FF	INTERRUPT CONTROLLER No. 1
011100–0111FF	INTERRUPT CONTROLLER No. 2
011200–0112FF	NETWORK ID PROM
011300–0113FF	LATCH-PAGE-ON-PARITY-ERROR REGISTER
011400 0114FF	MEMORY PRESENT REGISTER
011600–0116FF	MASTER REQUEST REGISTER
016400–0164FF	SELECTIVE CLEAR LOCATIONS [1]
017000–017FFF	ADDRESS TRANSLATION MAP
040000–05FFFF	AT BUS-COMPATIBLE I/O SPACE
060000–07FFFF	NOT USED

Physical Address	Function
080000–09FFFF	AT BUS-COMPATIBLE MEMORY SPACE OR ETHERCONTROLLER-AT MEMORY SPACE (80000 - 84000; ALTERNATE = 81FFF - 85FFF)
0A0000–0BFFFF	COLOR OR ALTERNATE MONO GRAPHICS MEMORY SPACE
0C0000–0DFFFF	ALTERNATE MONO GRAPHICS MEMORY SPACE OR SINGLE-BOARD RING CONTROLLER MEMORY SPACE (D0000 - DFFFF)
0E0000–0FFFFF	ALTERNATE COLOR GRAPHICS MEMORY SPACE OR ALTERNATE SINGLE-BOARD RING CONTROLLER MEMORY SPACE (E0000 - EFFFF)
100000–FFFFFF	AT COMPATIBLE BUS MEMORY SPACE
FA0000–FDFFFF	MONO GRAPHICS MEMORY SPACE
FE0000–FFFFFF	AT COMPATIBLE BUS MEMORY SPACE
1000000–1FFFFFF	MAIN MEMORY (16 MB)
2000000–2FFFFFF	MAIN MEMORY (16 MB)
3000000–3FFFFFF	MAIN MEMORY (16MB)
4000000–4FFFFFF	MAIN MEMORY (16MB)
5000000–6FFFFFF	RESERVED
7000000–700FFFF	I/O PROTECTION MAP
7010000–F7FFFFFF	RESERVED
F8000000–FDFFFFFF	DESKTOP VISUALIZATION SPACE

[1] Selective Clear Locations:

Physical Address	Function
00016400	Clear All Locations
00016404	Clear FPU Trap
00016406	Clear Parity Error Flag
00016408	Clear Bus Error Status
0001640A	Clear Graphics Trap

On pages 4–10 and 4–11, replace section 4.2.1.4 with the following information.

4.2.1.4 DS3500, DS4000, DS4500, and DS5500 Address Translation Map

The Address Translation Map exists in the DS3500, DS4000, DS4500, and DS5500. The map has the following two functions:

- It allows the DS3500, DS4000, DS4500, or DS5500 to perform DMA to or from noncontiguous physical memory (while it appears that the DMA transfer is taking place from contiguous physical memory)
- It provides a 512–KB window through which external AT compatible bus masters can access CPU main memory.

The Address Translation Map holds one entry for every main memory page that is accessed via a DMA controller or other external AT compatible bus master. The operating system allocates an Address Translation Map entry (or multiple entries) each time DMA is required. The map provides the interface between the DMA controller 64–KB (for 8–bit transfers) or 128–KB (for 16–bit transfers) address spaces and the DS3500 or DS4000 physical address space (64 MB).

When an external bus master assumes control of the AT compatible bus, the physical address space between addresses **000000** and **07FFFF** is used by the Address Translation Map to access the 64– to 128–KB bus master's address space.

During 8–bit DMA transfers in the DS3500, DS4000, DS4500, and DS5500, address bits **<15:10>** provide an index into the Address Translation Map; they select one of the 64 entries contained within it. The 16–bit Address Translation Map entry (a physical page number, bits **<25:10>**) is concatenated with the page offset (DMA address bits **<9:0>**), which yields a 26–bit physical address.

During 16–bit DMA transfers in the DS3500, DS4000, DS4500, and DS5500, address bits **<16:10>** provide an index into the Address Translation Map; they select one of the 128 entries contained within it. The 16–bit Address Translation Map entry (a physical page number, bits **<25:10>**) is concatenated with the page offset (DMA address bits **<9:1>**), which yields a 26–bit physical address.

For more information about DMA on the AT compatible bus, refer to Subsection 4.3.3.

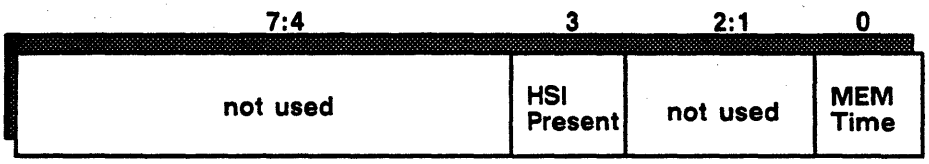
On page 4–19, add the following line to Table 4–6.

PC ON/OFF	Physical Cache (DS4500 Only)

On page 4–24, Replace the information in section 4.2.1.14 with the following information.

4.2.1.14 DS5500 Cache Status Register

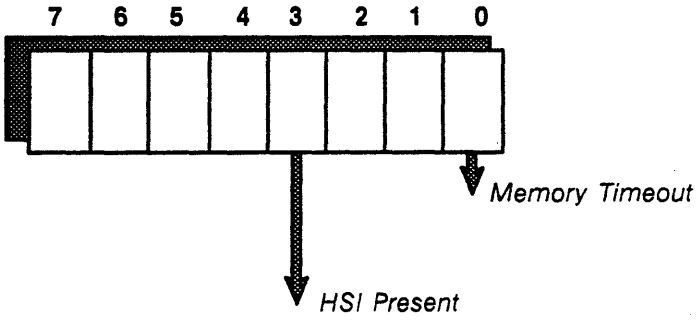
This 8-bit, read-only register exists in the DS5500. This register holds miscellaneous status information. Figure 4–9 and Figure 4–10 show the register.



HSI Present <3>
This bit is cleared (0) to indicate that a graphics device is in the HSI connector.

MEM Time <0>
This bit indicates an access to non-existant memory.

Figure 4–9. DS5500 Cache Status Register



HSI Present <3>
This bit is cleared (0) to indicate that a graphics device is in the HSI connector.

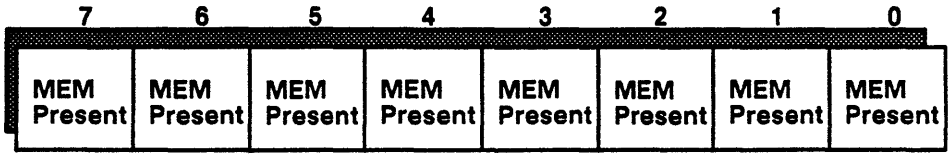
MEM Time <0>
This bit indicates an access to non-existant memory.

Figure 4–10. DS5500 Cache Status Register

On page 4–26, after section 4.2.1.17, add the following section .

4.2.1.18 DS5500 Memory Present Register

This 8-bit, read-only register exists in the DS5500. This register holds memory board existence information. The following figure shows the register.



MEM Present <7-0>
These bits are cleared (0) when memory boards are present.

In this register, each consecutive pair of bits identifies the condition of a memory board slot. Bits 0 and 1 are slot 0, bits 2 and 3 are slot 1, bits 4 and 5 are slot 2, and bits 6 and 7 are slot 3.

The locations of memory board slots on the CPU Motherboard is as follows:

- Slot 0 is location P25 on the CPU Motherboard (Right-most slot)
- Slot 1 is location P24 on the CPU Motherboard
- Slot 2 is location P23 on the CPU Motherboard
- Slot 3 is location P22 on the CPU Motherboard (Left-most slot)

The following table shows the hexadecimal value of the Memory Present register for all possible memory configurations.

Memory Bd. Size (MB)		Memory Bd. Size (MB)	
Slot No. 0 1 2 3	**Register value (Hexadecimal)**	**Slot No. 0 1 2 3**	**Register value (Hexadecimal)**
(No Board)	FF	16 4 4 4	A9
4 – – –	FE	16 8 – –	F1
4 4 – –	FA	16 8 4 –	E1
4 4 4 –	EA	16 8 4 4	A1
4 4 4 4	AA	16 8 8 –	C1
8 – – –	FC	16 8 8 4	81
8 4 – –	F8	16 8 8 8	01
8 4 4 –	E8	16 16 – –	F5
8 4 4 4	A8	16 16 4 –	E5
8 8 – –	F0	16 16 4 4	A5
8 8 4 –	E0	16 16 8 –	C5
8 8 4 4	A0	16 16 8 4	85
8 8 8 –	C0	16 16 8 8	05
8 8 8 4	80	16 16 16 –	D5
8 8 8 8	00	16 16 16 4	95
16 – – –	FD	16 16 16 8	15
16 4 – –	F9	16 16 16 16	55
16 4 4 –	E9		


0 1 5 4 1 1 - A 0 0